WHAT IS CLAIMED IS:

1. A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin port configured to produce said signal; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein:

said signal is capable of being represented as a series of characters, and a character of said series of characters is capable of being represented as a first data bit, a second data bit, and a first control bit;

a first interconnect of said set of interconnects is configured to convey said first data bit, a second interconnect of said set of interconnects is configured to convey said second data bit, and a third interconnect of said set of interconnects is configured to convey said first control bit; and

said first interconnect, said second interconnect, and said third interconnect are configured in a manner to reduce cross-talk.

2. The cross link multiplexer bus of claim 1, wherein said third interconnect is positioned substantially between said first interconnect and said second interconnect.

3. The cross link multiplexer bus of claim 2, wherein said first interconnect, said second interconnect, and said third interconnect are fabricated on a common layer within an integrated circuit chip, said common layer substantially defined by a plane.

4. The cross link multiplexer bus of claim 2, wherein:

said series of characters is further capable of being represented as a third data bit, a fourth data bit, and a second control bit;

a fourth interconnect of said set of interconnects is configured to convey said third data bit, a fifth interconnect of said set of interconnects is configured to convey said fourth data bit, and a sixth interconnect of said set of interconnects is configured to convey said second control bit; and

said sixth interconnect is positioned substantially between said fourth interconnect and said fifth interconnect.

5. The cross link multiplexer bus of claim 4, wherein said first interconnect, said second interconnect, said third interconnect, said fourth interconnect, said fifth interconnect, and said sixth interconnect are fabricated on a common layer within an integrated circuit chip, said common layer substantially defined by a plane.

6. The cross link multiplexer bus of claim 4, wherein:

said first interconnect, said second interconnect, and said third interconnect are fabricated on a first layer within an integrated circuit chip, said first layer substantially defined by a first plane; and

said fourth interconnect, said fifth interconnect, and said sixth interconnect are fabricated on a second layer within said integrated circuit chip, said second layer substantially defined by a second plane, said second plane substantially parallel to said first plane.

7. The cross link multiplexer bus of claim 6, wherein:

said fourth interconnect is positioned substantially adjacent to said third interconnect along a direction substantially perpendicular to said first plane and said second plane; and

said sixth interconnect is positioned substantially adjacent to said second interconnect along said direction substantially perpendicular to said first plane and said second plane.

8. A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal, an origin port configured to produce said signal, a first power supply configured to provide a first voltage, and a second power supply configured to provide a second voltage, said first voltage different from said second voltage; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein:

said signal is capable of being represented as a series of characters, and a character of said series of characters is capable of being represented as a first bit and a second bit;

a first interconnect of said set of interconnects is configured to convey said first bit, a second interconnect of said set of interconnects is configured to convey said second bit, and a third interconnect of said set of interconnects is configured to convey one of said first voltage and said second voltage; and

said first interconnect, said second interconnect, and said third interconnect are configured in a manner to reduce cross-talk.

9. The cross link multiplexer bus of claim 8, wherein said third interconnect is positioned substantially between said first interconnect and said second interconnect.

10. The cross link multiplexer bus of claim 9, wherein said first interconnect, said second interconnect, and said third interconnect are fabricated on a common layer within an integrated circuit chip, said common layer substantially defined by a plane.

11. The cross link multiplexer bus of claim 9, wherein:

said series of characters is further capable of being represented as a third bit and a fourth data bit;

a fourth interconnect of said set of interconnects is configured to convey said third bit, a fifth interconnect of said set of interconnects is configured to convey said fourth bit, and a sixth interconnect of said set of interconnects is configured to convey one of said first voltage and said second voltage; and

said sixth interconnect is positioned substantially between said fourth interconnect and said fifth interconnect.

12. The cross link multiplexer bus of claim 11, wherein said first interconnect, said second interconnect, said third interconnect, said fourth interconnect, said fifth interconnect, and said sixth interconnect are fabricated on a common layer within an integrated circuit chip, said common layer substantially defined by a plane.

13. The cross link multiplexer bus of claim 11, wherein:

said first interconnect, said second interconnect, and said third interconnect are fabricated on a first layer within an integrated circuit chip, said first layer substantially defined by a first plane; and

said fourth interconnect, said fifth interconnect, and said sixth interconnect are fabricated on a second layer within said integrated circuit chip, said second layer substantially defined by a second plane, said second plane substantially parallel to said first plane.

14. The cross link multiplexer bus of claim 13, wherein:

said fourth interconnect is positioned substantially adjacent to said third interconnect along a direction substantially perpendicular to said first plane and said second plane; and

said sixth interconnect is positioned substantially adjacent to said second interconnect along said direction substantially perpendicular to said first plane and said second plane.

15. In a cross link multiplexer bus having a plurality of substantially parallel interconnects coupled between a pair of adjacent cross link multiplexers, a method for reducing cross-talk, comprising the steps of:

(1) conveying a first bit of a character of a signal though a first interconnect of the plurality of substantially parallel interconnects;

(2) conveying a second bit of the character of the signal though a second interconnect of the plurality of substantially parallel interconnects; and

(3) conveying a power supply voltage though a third interconnect of the plurality of substantially parallel interconnects;

wherein said third interconnect is positioned substantially between said first interconnect and said second interconnect.

16. The method of claim 15, wherein the power supply voltage is a ground.

17. In a cross link multiplexer bus having a plurality of substantially parallel interconnects coupled between a pair of adjacent cross link multiplexers, a method for reducing cross-talk, comprising the steps of:

(1) conveying a first data bit of a character of a signal though a first interconnect of the plurality of substantially parallel interconnects;

(2) conveying a second data bit of the character of the signal though a second interconnect of the plurality of substantially parallel interconnects; and

(3) conveying a control bit of the character of the signal though a second interconnect of the plurality of substantially parallel interconnects;

wherein said third interconnect is positioned substantially between said first interconnect and said second interconnect.